Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **NOT 1Q**
2. **1D**
3. **2D**
4. **3C,4C**
5. **VCC**
6. **3D**
7. **4D**
8. **NOT 4Q**
9. **4Q**
10. **3Q**
11. **NOT 3Q**
12. **GND**
13. **1C,2C**
14. **NOT 2Q**
15. **2Q**
16. **1Q**

**.046”**

**.0525”**

**2 1 16 15 14**

**13**

**12**

**3**

**4**

**5**

**6 7 8 9 10 11**

**75**

**MASK REF**

**A**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: NO CONNECT**

**Mask Ref: 75 A**

**APPROVED BY: DK DIE SIZE .046” X .052” DATE: 6/7/18**

**MFG: T.I. / NATIONAL THICKNESS .025” P/N: 54LS75**

**DG 10.1.2**

#### Rev B, 7/19/02